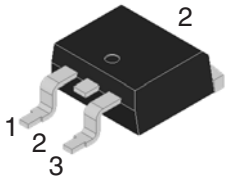
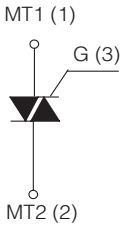
# LOGIC LEVEL TRIAC

## TO-263AB (D2PAK)




**On-State Current**
12 Amp

**Gate Trigger Current**
≤ 10 mA

**Off-State Voltage**
400 V ÷ 800 V

**FEATURES**

- Glass/passivated die junctions
- Medium current Triac
- Ideal for automated placement
- Low thermal resistance
- High surge current capability
- Low forward voltage drop
- Solder dip 260°C, 10s
- Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC
- Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C

Pb

e3

**RoHS** COMPLIANT

**MECHANICAL DATA**

- **Case:** TO-263AB (D2PAK). Epoxy meets UL 94V-0 flammability rating.
- **Polarity:** As marked on the body.
- **Terminals:** Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.

**TYPICAL APPLICATIONS**

Logic level versions are designed to interface directly with low power drivers such as microcontrollers.

## Maximun Ratings and Electrical Characteristics at 25°C

| SYMBOL | PARAMETER | CONDITIONS | Value | Unit |
|---|---|---|---|---|
| $I_{T(RMS)}$ | RMS On-state Current (full sine wave) | All Conduction Angle, $T_C$ =95 °C | 12 | A |
| $I_{TSM}$ | Non-repetitive On-State Current | Full Cycle, 60 Hz (t = 16.7 ms) | 110 | A |
| $I_{TSM}$ | Non-repetitive On-State Current | Full Cycle, 50 Hz (t = 20 ms) | 100 | A |
| $I^2t$ | Fusing Current | tp = 10 ms, Half Cycle | 50 | $A^2s$ |
| $I_{GM}$ | Peak Gate Current | 20 µs max. $T_j$ = 125 °C | 4 | A |
| $P_{G(AV)}$ | Average Gate Power Dissipation | $T_j$ = 125 °C | 1 | W |
| dI/dt | Critical rate of rise of on-state current | $I_G$ = 2x $I_{GT}$, $t_r$ ≤100ns<br>f = 120 Hz, $T_j$ = 125 °C | 50 | A/µs |
| $T_j$ | Operating Temperature | | (-40 +125) | °C |
| $T_{stg}$ | Storage Temperature | | (-40 +150) | °C |
| $T_{sld}$ | Soldering Temperature | 10s max | 260 | °C |

| SYMBOL | PARAMETER | VOLTAGE | | | Unit |
|---|---|---|---|---|---|
| | | D | M | N | |
| $V_{DRM}/V_{RRM}$ | Repetitive Peak Off State Voltage | 400 | 600 | 800 | V |

# LOGIC LEVEL TRIAC

## Electrical Characteristics at Tamb = 25 °C

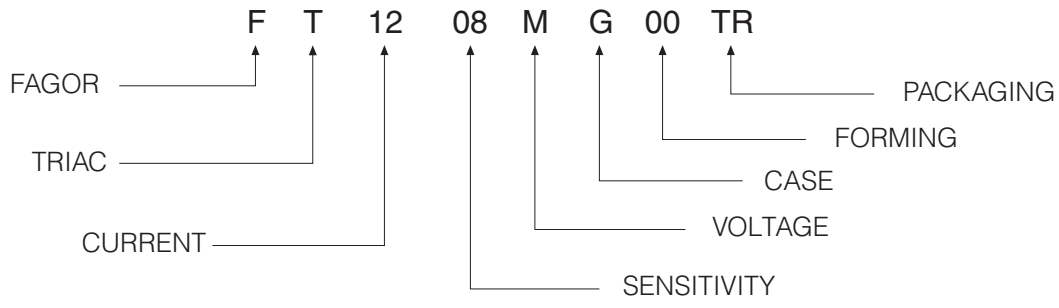
| SYMBOL | PARAMETER | CONDITIONS | Quadrant | | SENSITIVITY | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | 04 | 08 | 09 | |
| $I_{GT}$ (1) | Gate Trigger Current | $V_D$ = 12 $V_{DC}$, $R_L$ = 33 Ω, $T_j$ = 25 °C | Q1÷Q3 | MAX | 5 | 10 | 10 | mA |
| | | | Q4 | MAX | - | | 10 | mA |
| $V_{GT}$ | Gate Trigger Voltage | $V_D$ = 12 $V_{DC}$, $R_L$ = 33 Ω, $T_j$ = 25 °C | Q1÷Q3 | MAX | 1.3 | | | V |
| | | | Q1÷Q4 | MAX | 1.3 | | | V |
| $V_{GD}$ | Gate Non Trigger Voltage | $V_D$ = $V_{DRM}$, $R_L$ = 3.3 KΩ, $T_j$ = 125 °C | Q1÷Q3 | MIN | 0.2 | | | V |
| | | | Q1÷Q4 | MIN | 0.2 | | | V |
| $I_H$ (2) | Holding Current | $I_T$ = 100 mA, Gate open, $T_j$ = 25 °C | | MAX | 15 | 15 | 20 | mA |
| $I_L$ | Latching Current | $I_G$ = 1.2 $I_{GT}$, $T_j$ = 25 °C | Q1,Q3 | MAX | 25 | 25 | | mA |
| | | | Q1,Q3,Q4 | MAX | | | 20 | mA |
| | | | Q2 | MAX | 30 | 30 | 25 | mA |
| dV/dt (2) | Critical Rate of Voltage Rise | $V_D$ = 0.67 x $V_{DRM}$, Gate open $T_j$ = 125 °C | | MIN | 40 | 40 | 40 | V/µs |
| (dI/dt)c (2) | Critical Rate of Current Rise | (dv/dt)c = 0.1 V/µs $T_j$ = 125 °C | | MIN | 5.4 | 6.5 | 2.5 | A/ms |
| | | (dv/dt)c = 10 V/µs $T_j$ = 125 °C | | MIN | 2.8 | 2.9 | 1.5 | A/ms |
| | | without snubber $T_j$ = 125 °C | | MIN | - | - | - | |
| $V_{TM}$ (2) | On-state Voltage | $I_T$ = 17 Amp, tp = 380 µs, $T_j$ = 25 °C | | MAX | 1.55 | | | V |
| $V_{to}$ (2) | Threshold Voltage | $T_j$ = 125 °C | | MAX | 0.85 | | | V |
| $r_d$ (2) | Dynamic resistance | $T_j$ = 125 °C | | MAX | 70 | | | mΩ |
| $I_{DRM}/I_{RRM}$ | Off-State Leakage Current | $V_D$ = $V_{DRM}$, $T_j$ = 125 °C | | MAX | 1 | | | mA |
| | | $V_R$ = $V_{RRM}$, $T_j$ = 25 °C | | MAX | 5 | | | µA |
| $R_{th(j-c)}$ | Thermal Resistance Junction-Case | for AC 360° conduction angle | | | 1.3 | | | °C/W |
| $R_{th(j-a)}$ | Thermal Resistance Junction-Ambient | S(3) = 1 $cm^2$ | | | 45 | | | °C/W |

(1) Minimum $I_{GT}$ is guaranted at 5% of $I_{GT}$ max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

(3) S: Cooper surface under tab.

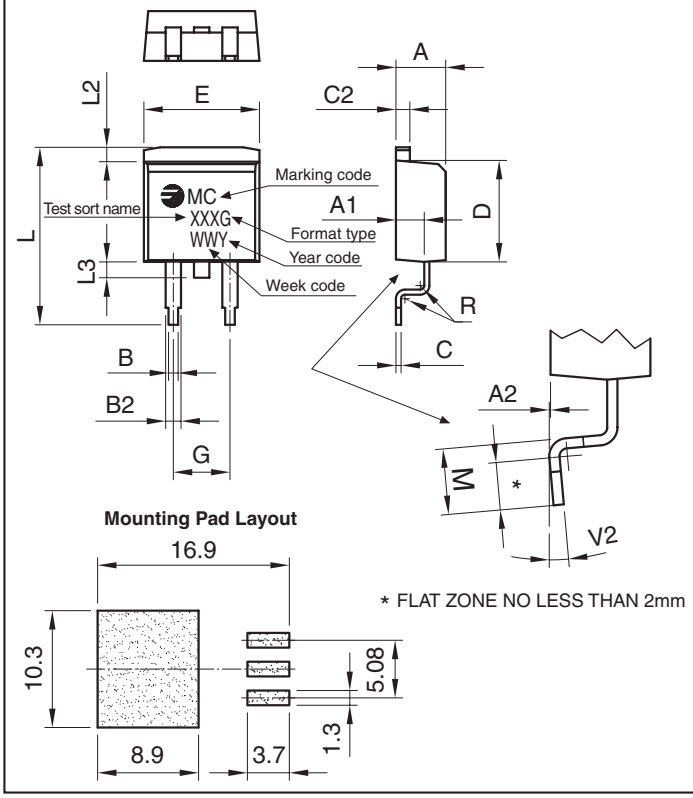
## Part Number Information



## Ordering information

| PREFERRED P/N | PACKAGE CODE | DELIVERY MODE | BASE QUANTITY | UNIT WEIGHT (g) |
|---|---|---|---|---|
| FT1209MG 00TR | TR | 13" diameter tape and reel | 800 | 1.50 |

## Package Outline Dimensions: (mm) TO-263AB (D2PAK)




| REF. | DIMENSIONS | | |
|---|---|---|---|
| | Milimeters | | |
| | Min. | Nominal | Max. |
| A | 4.40 | 4.45 | 4.60 |
| A1 | 2.49 | 2.50 | 2.69 |
| A2 | 0.03 | 0.10 | 0.23 |
| B | 0.70 | 0.90 | 0.93 |
| B2 | 1.14 | 1.03 | 1.70 |
| C | 0.45 | 0.45 | 0.60 |
| C2 | 1.23 | 1.23 | 1.36 |
| D | 8.95 | 9.00 | 9.35 |
| E | 10.00 | 10.25 | 10.40 |
| G | 4.88 | 5.15 | 5.28 |
| L | 15.00 | 15.40 | 15.85 |
| L2 | 1.27 | 1.27 | 1.40 |
| L3 | 1.40 | 1.55 | 1.75 |
| M | 2.40 | 3.00 | 3.20 |
| R | | 0.40 typ | |
| V2 | 0º | | 8º |

## **Ratings and Characteristics** (Ta 25 ºC unless otherwise noted)

Fig. 1: Maximum power dissipation versus RMS on-state curren (full cycle).

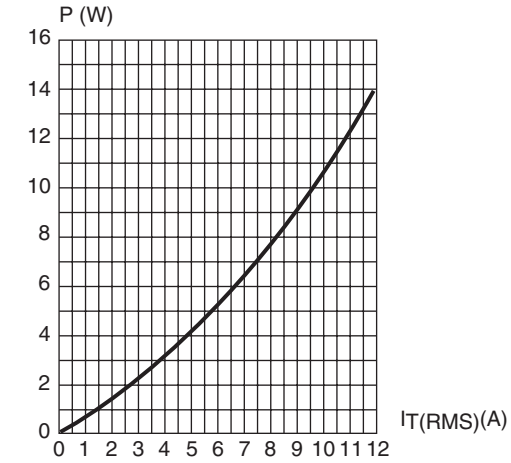



Fig. 2: RMS on-state current versus case temperature (full cycle).

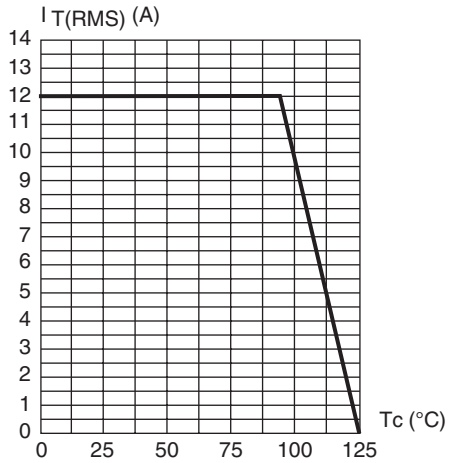



Fig. 3: Relative variation of thermal impedance versus pulse duration.

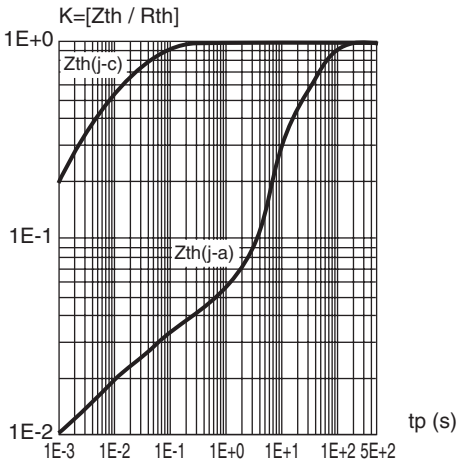



Fig. 4: On-state characteristics (maximum values)

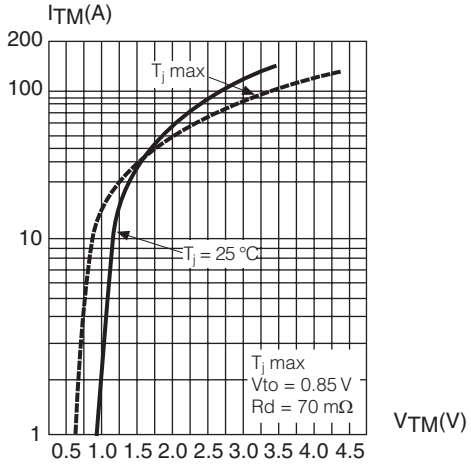



Fig. 5: Surge peak on-state current versus number of cycles

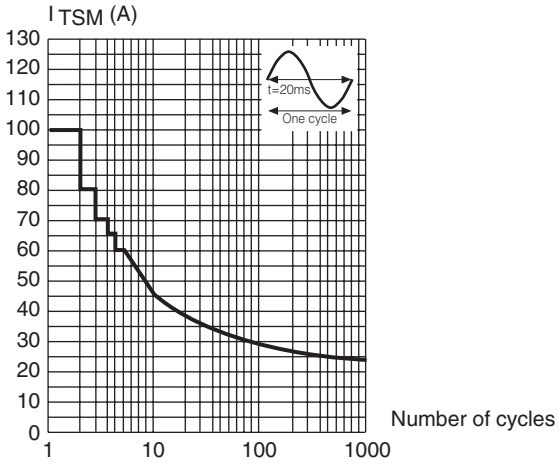
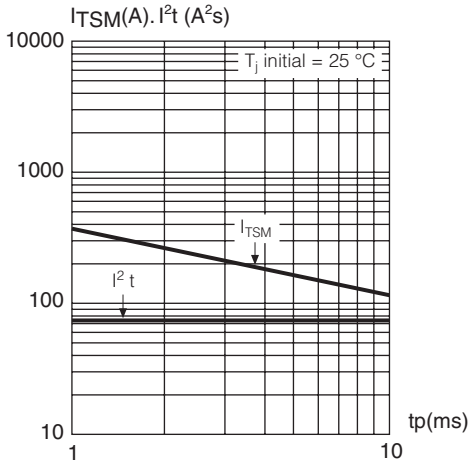



Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<10ms, and corresponding value of $I^2t$.



## **Ratings and Characteristics** (Ta 25 ºC unless otherwise noted)

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

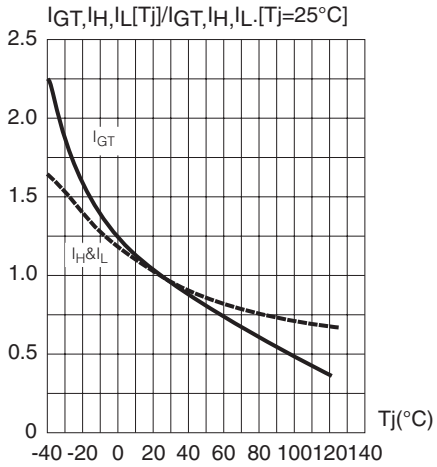



Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

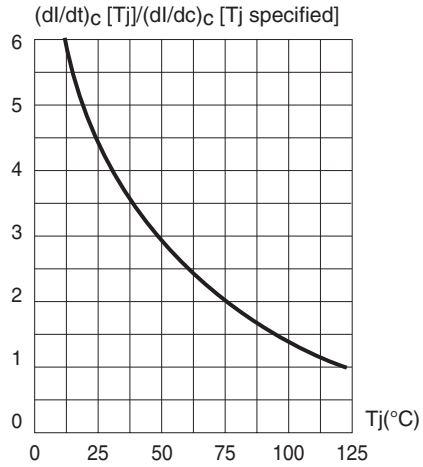



Fig. 9: Relative variation of critical rate of decrease of main current versus

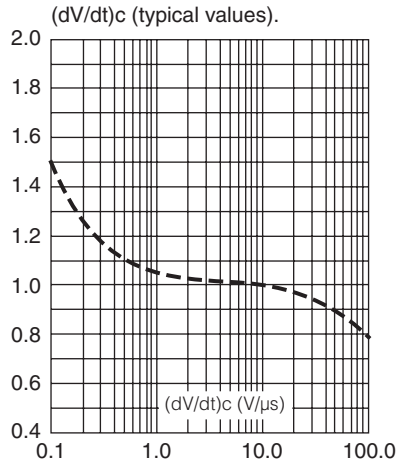
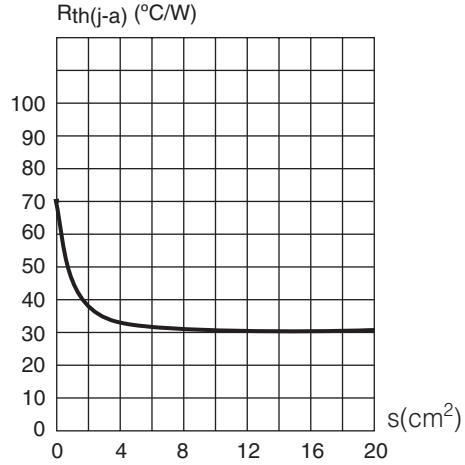



Fig. 10: D2PAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board copper thickness: 35µ)



**Revision History**

| Date | Revision | Description of Changes |
|---|---|---|
| 14-Feb-2012 | 0 | Original Data Sheet |
| 15-Jan-2014 | 1 | 200V and 700V eliminated & Add sensitivity 04 |

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